Reliability evaluation for

MDmesh™ DM2 Technology 8" Wafer Front-end Capacity Extension - Ang Mo Kio (Singapore) - AUTOMOTIVE

Process change

General Information	
Commercial Product	*: STW50N65DM2AG STW65N65DM2AG STW72N60DM2AG*
Product Line	*:* FQFIA1 – FQF9A1 – FQ69A1
Product Description	*:* Power MOSFET
Package	*:* TO-247
Silicon Technology	: MDmesh™ DM2
Division	*:Power Transistor Division*

Traceability	
Diffusion Plant	: SG8" (Singapore)
Assembly Plant	: ST Shenzhen (China)
Reliability Lab	: Catania (Italy)

Reliability Assessment	
Passed	☒

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	12 February 2019	A.SETTINIERI	FINAL REPORT

APPROVED BY:
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1. RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Reliability evaluation MDmesh™ DM2 Technology 8" Wafer Front-end Capacity Extension - Ang Mo Kio (Singapore) - AUTOMOTIVE

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with ZVEI Guidelines and are listed in the Test Plan.
For details on test conditions, generic data used and spec reference see test results summary at Par.3 .

#	Stress	Abrv	Reference	Data type	Test flag	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	1	Y	
2	External Visual	EV	JESD22B-101	1	Y	
3	Parametric Verification	PV	User specification	1	Y	
4	High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A	1	Y	
5	High Temperature Gate Bias	HTGB	JESD 22A-108	1	Y	
6	Temperature Cycling	TC	JESD22A-104	1	Y	
6a	Temperature Cycling Hot Test	TCHT	JESD22A-104	1	Y	
6a alt	TC Delamination Test	TCDT	JESD22A-104	1	Y	
7	Autoclave	AC	JESD22A-102	1	Y	
8	High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	1	Y	
9	Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	1	Y	
10	ESD Characterization	ESD (HBM,CDM)	AEC Q101-001 and 005	1	Y	
11	Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	1	Y	
12	Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	3	Y	
13	Wire Bond Strength	WBS	MIL-STD-750 Method 2037	3	Y	
14	Bond Shear	BS	AEC-Q101-003	3	Y	
15	Die Shear	DS	MIL-STD-750 Method 2017	3	Y	
16	Dielectric Integrity	DI	AEC-Q101-004 section 3	3	Y	

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die and package oriented test showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.
ESD is accordance with ST spec.

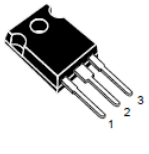
On the basis of the overall results obtained, we can give a positive judgment on the reliability evaluation for MDmesh™ DM2 Technology 8" Wafer Front-end Capacity Extension for Automotive product diffused in SG8" (Singapore) Fab and assembled in ST Shenzhen (China) in agreement with ZVEI Guidelines.

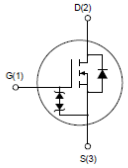
2. DEVICE/TEST VEHICLE CHARACTERISTICS

2.1 Generalities

Power MOSFET MDmesh™ DM2

2.2 Pin Connection





2.3 Traceability

Reference "Product Baseline" document if existing, else provide following chapters/information:

D.U.T.: STW50N65DM2AG PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	7510 x 5760 µm^2
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO-247 3L Selected Ni/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate: Al/Mg 5 mils - Source: Al 15mils
Molding compound	Halogen Free

D.U.T.: STW65N65DM2AG PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10390 x 6850 μm^2
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO-247 3L Selected Ni/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate: Al/Mg 5 mils - Source: Al 10mils
Molding compound	Halogen Free

D.U.T.: STW72N60DM2AG PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10390 x 6850 μm^2
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO-247 3L Selected Ni/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate: Al/Mg 5 mils - Source: Al 10mils
Molding compound	Halogen Free

Reliability Testing Information	
Reliability laboratory location	Catania (Italy)
Electrical testing location	Catania (Italy)

3. TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Commercial Product	Product line	Package	Wafer Fab	Assembly plant	Note
1	STW50N65DM2AG	FQFIA1	TO-247	SG8" (Singapore)	ST Shenzhen (China)	
2	STW65N65DM2AG	FQF9A1				
3	STW72N60DM2AG	FQ69A1				

3.2 Test results summary

Test	Std ref.	Conditions	SS	Steps	Failure/SS		
					Lot 1	Lot 2	Lot 3
TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.			462	462	462
External visual	JESD22 B-101	All devices submitted for testing			462	462	462
Parametric Verification	User specification	All parameters according to user specification from -55°C to 175°C		75	25	25	25
Silicon oriented tests							
HTRB	MIL-STD-750-1 M1038 Method A	Tj = 150°C, BIAS = 520V	154	1000 h	0/77	0/77	
		Tj = 150°C, BIAS = 600V	77				0/77
HTGB	JESD22 A-108	Tj = 150°C, BIAS = 30V	231	1000 h	0/77	0/77	0/77
Package oriented Tests							
TC	JESD22 A-104	TA=-55°C TO 150°C	231	1000cy	0/77	0/77	0/77
AC	JESD22 A-102	TA=121°C ; PA=2ATM	231	96h	0/77	0/77	0/77
H3TRB	JESD22 A-101	TA=85°C ; RH=85% BIAS= 100V	231	1000 h	0/77	0/77	0/77
IOL	MIL-STD-750 Method 1037	ΔTj ≥100°C	231	15Kcy	0/77	0/77	0/77
ESD	AEC Q101-001,002 and 005	CDM / HBM	60		0/30 0/30		
D.P.A.	AEC-Q101-004 Section 4	Devices after H3TRB - TC	4		0/2 0/2		
Thermal Resistance	JESD24-3, 24-4, 24-6 as appropriate		10 each Pre-post change		0/10		
Wire Bond Strength	MIL-STD-750 Method 2037		10 bonds from min of 5 devices		0/5		
Bond Shear	AEC-Q101-003		10 bonds from min of 5 devices 5		0/5		
Die Shear	MIL-STD-750 Method 2017		5		0/5		
Dielectric Integrity	AEC-Q101-004 section 3		5		0/5		

Catania, February 14 2019

Automotive Discrete Group (ADG)
Power Transistor Division
HV Business Unit
Process Change Notification

MDmesh™ DM2 Technology Power MOSFET Transistors 8" Wafer Front-end Capacity Extension Ang Mo Kio AUTOMOTIVE

Dear Customer,

Following the continuous improvement of our service and in order to increase Front-end Capacity, this document is announcing the new 8" wafer line for MDmesh™ DM2 Technology of Power MOSFET Transistors in ST's Ang Mo Kio (Singapore) FAB.

MDmesh™ DM2 Technology manufactured in 8" wafer size of Ang Mo Kio (Singapore) FAB, guarantees the same quality and electrical characteristics as per current production. This production is already born with front top metal AlCu+Ti/TiN barrier as per PCN ADG/18/11269 dated December 16 2018.

The involved product series are listed in the table below:

Product Family	Technology	Part Number
Power MOSFET Transistors	MDmesh™ DM2	STxxxN6xDM2AG

Any other Product related to the above series, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 08-2019.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistors	TO-247	STW50N65DM2AG STW65N65DM2AG STW72N60DM2AG

Change implementation schedule:

The production start and first shipments will be implemented after week 33 of 2019.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of 8" wafer size, manufactured in ST's Ang Mo Kio (Singapore) FAB, will be ensured by internal code (Finished Good) and Q.A. number.

Yours faithfully.